

*Fig. 1*  
*Prior Art*



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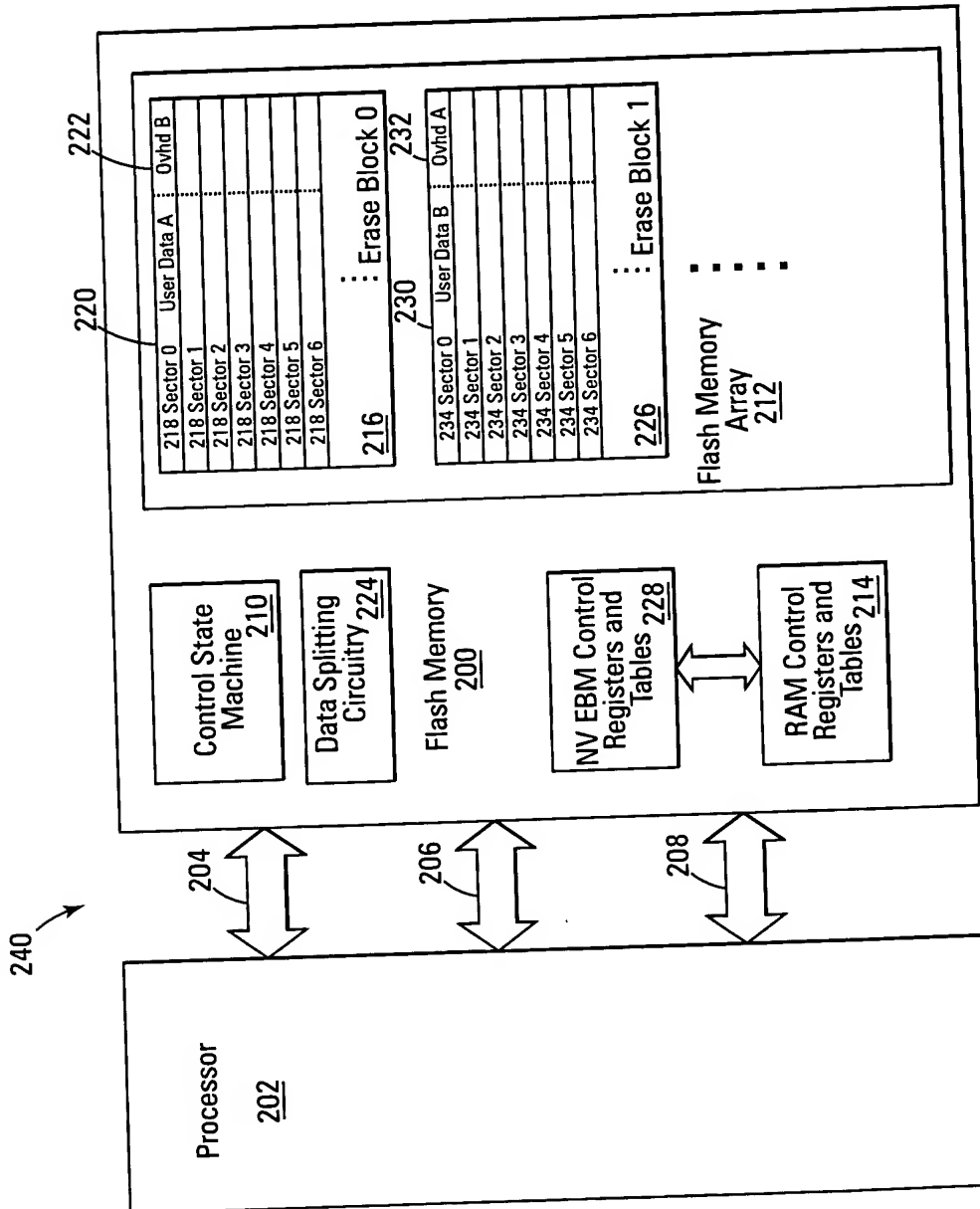


Fig. 2A



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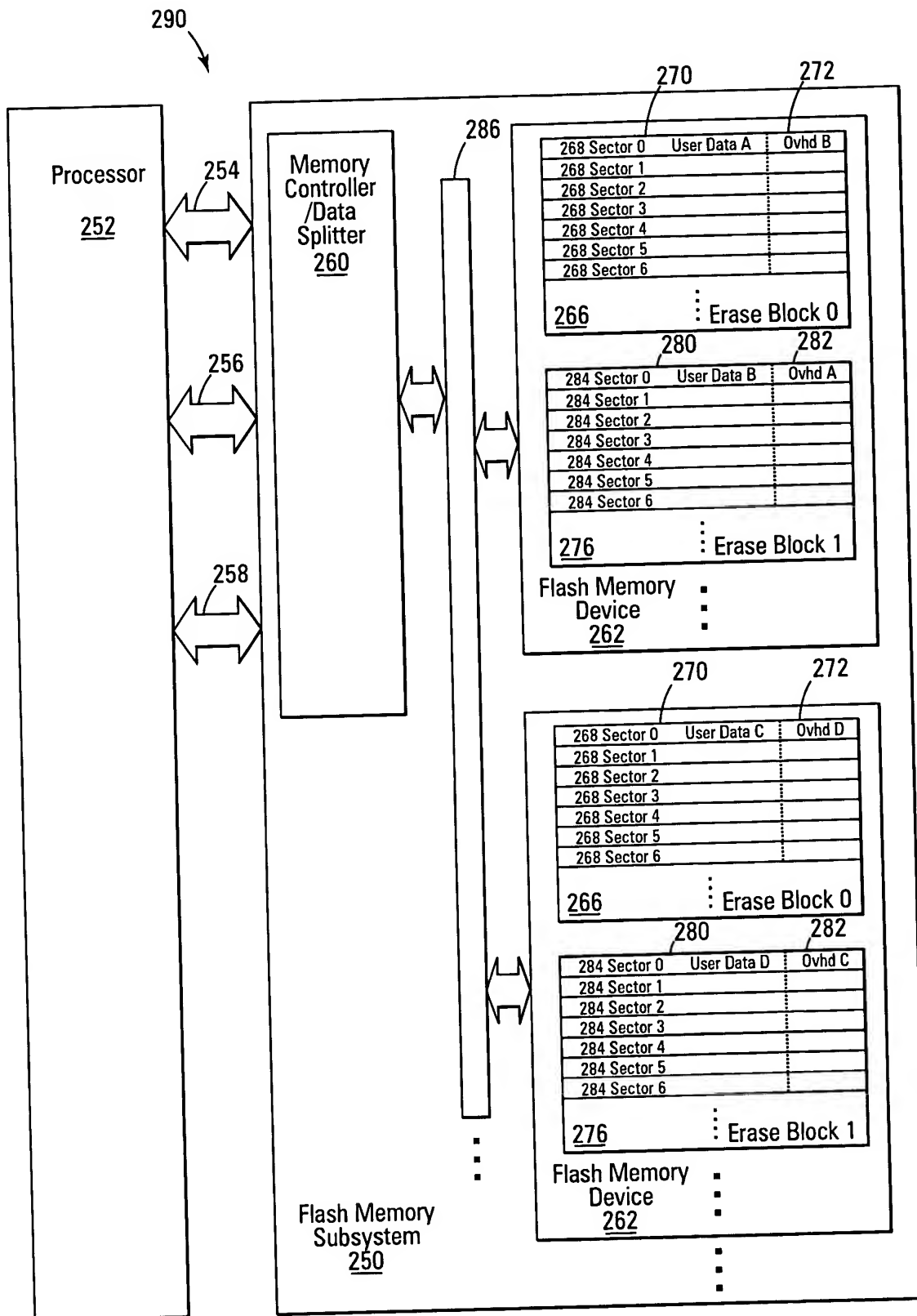


Fig. 2B

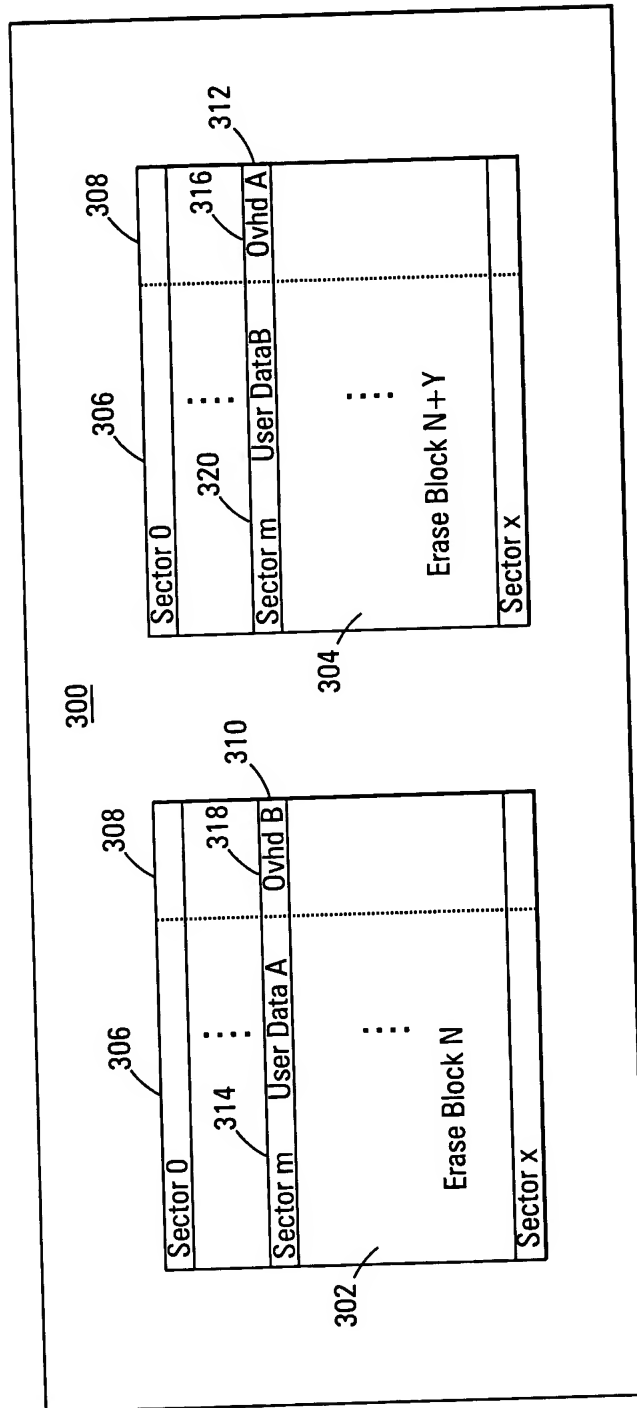


Fig. 3



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400		406	408	410	412	
{	414 Sector 0	1	4	414 Sector 0	3	2
	414 Sector 1	5	8	414 Sector 1	7	6
	414 Sector 2			414 Sector 2		
{	414 Sector 3		2	414 Sector 3	1	
	414 Sector 4	3	6	414 Sector 4	5	4
	414 Sector 5	7		414 Sector 5		8
	414 Sector 6			414 Sector 6		
	402	⋮	Erase Block N	404	⋮	Erase Block N+Y

Fig. 4A

450		456	458	460	462	
{	464 Sector 0	1	B	464 Sector 0	A	2
	464 Sector 1	3	D	464 Sector 1	C	4
	464 Sector 2	:	:	464 Sector 2	:	:
	464 Sector 3	:	:	464 Sector 3	:	:
	464 Sector 4			464 Sector 4		
	464 Sector 5			464 Sector 5		
	464 Sector 6			464 Sector 6		
	452	⋮	Erase Block N	454	⋮	Erase Block N+Y

Fig. 4B

470		476	478	480	482	
{	484 Sector 0	A	o/h P	484 Sector 0	B	o/h A
	484 Sector 1	C	o/h B	484 Sector 1	D	o/h C
	484 Sector 2	E	o/h D	484 Sector 2	F	o/h E
	484 Sector 3	:	:	484 Sector 3	:	:
	484 Sector 4	:	:	484 Sector 4	:	:
	484 Sector 5			484 Sector 5		
	484 Sector 6			484 Sector 6		
	472	⋮	Erase Block N	474	⋮	Erase Block N+Y
	484 Sector X-1	M	o/h K	484 Sector X-1	N	o/h M
	484 Sector X	O	o/h N	484 Sector X	P	o/h O

Fig. 4C



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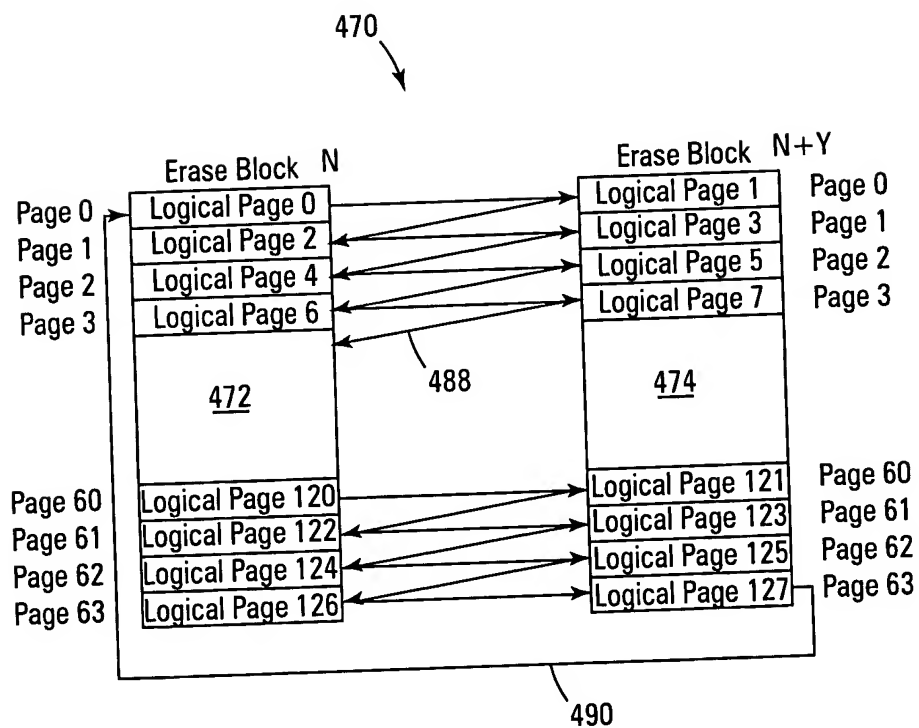


Fig. 4D



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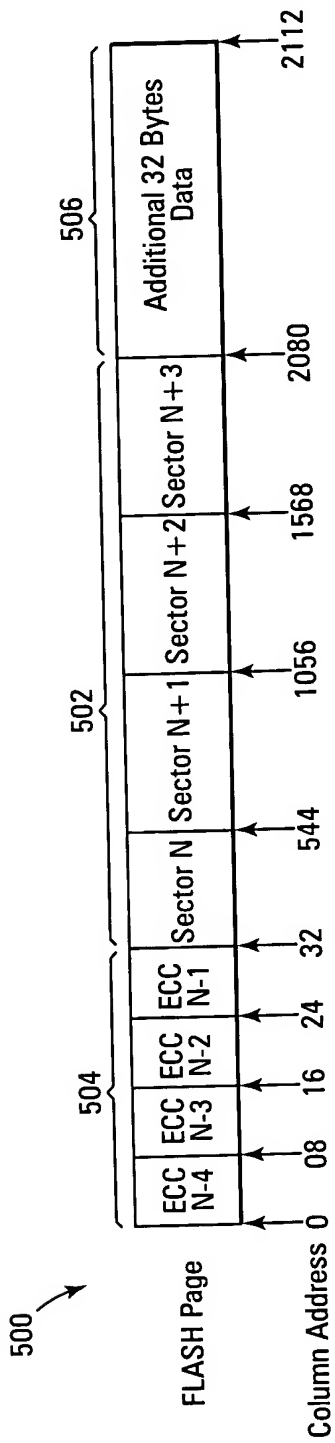


Fig. 5



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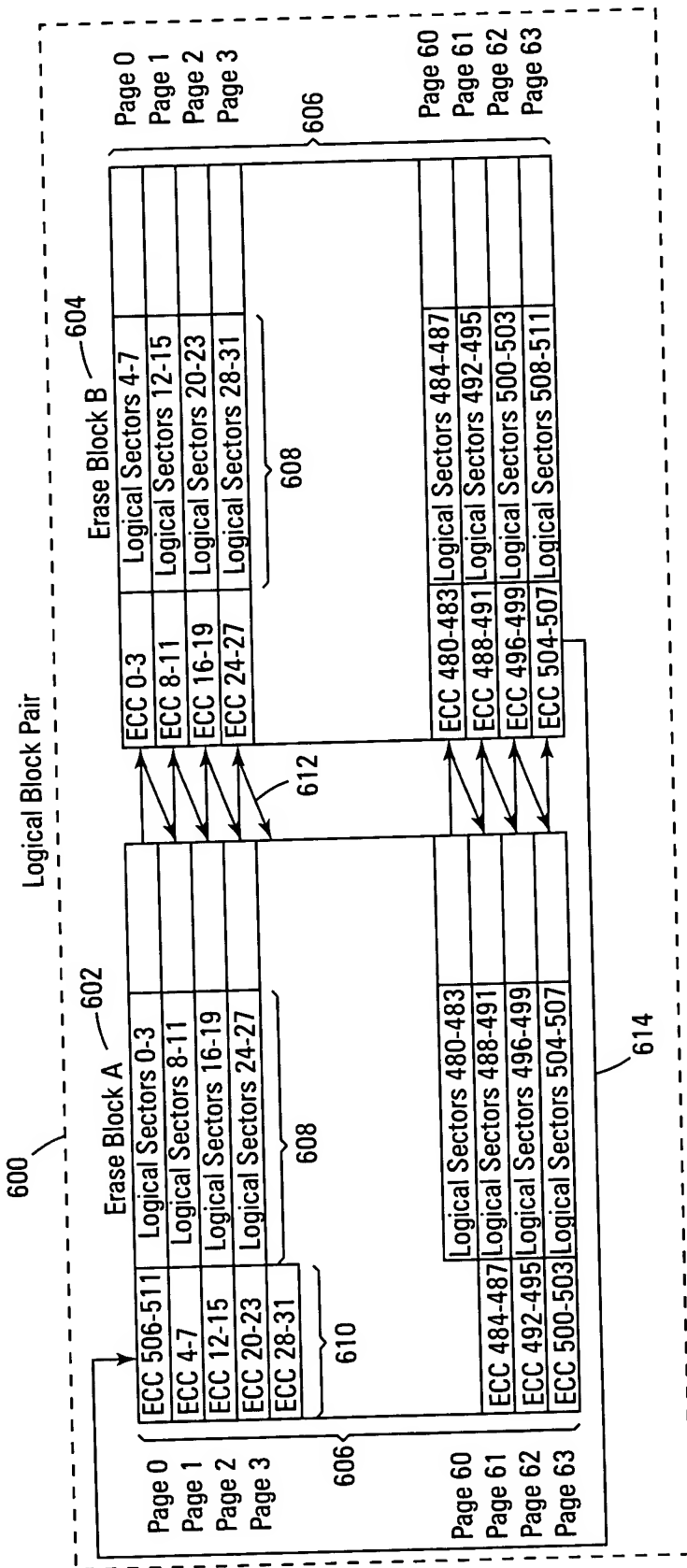


Fig. 6A



600

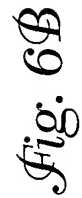


Fig. 6B



The diagram illustrates the internal structure of a NAND Flash Interface (700). It features a central **Control Circuitry** block (702) that manages the interface. The interface is divided into two main sections: **Register A** and **Register B**.

- Register A** (712) includes a **Zero Row** (724) and a **Regular Block Size** (726) section. It is connected to a **Microprocessor Load** (708) and a **Toggle** (706) signal.
- Register B** (716) includes a **Zero Column** (722) and a **Microprocessor Load** (708) section. It is connected to a **Microprocessor Load** (708) and a **Toggle** (706) signal.

The interface also includes a **Microprocessor Interface** (732) and a **NAND Flash Interface** (734). The **Microprocessor Interface** (732) is connected to the **Control Circuitry** (702) and the **Microprocessor Load** (708). The **NAND Flash Interface** (734) is connected to the **Control Circuitry** (702) and the **Microprocessor Load** (708).

Fig. 7



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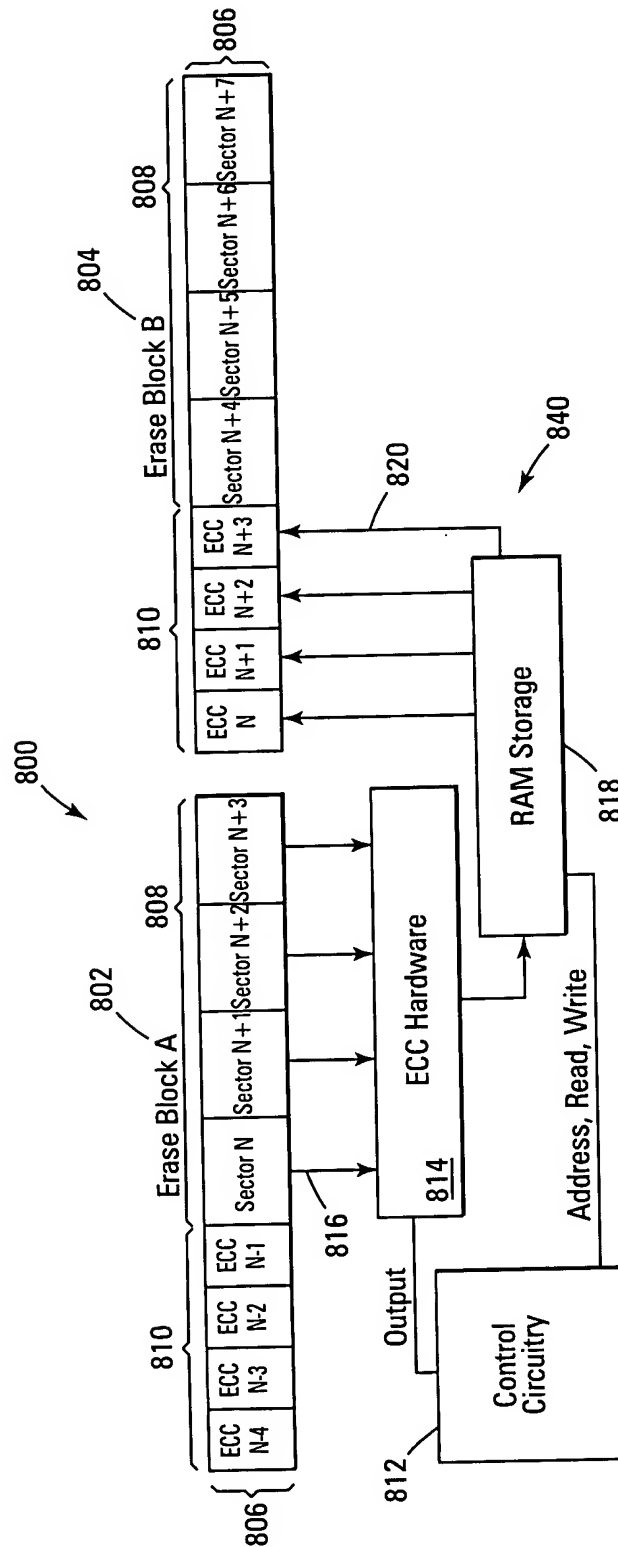


Fig. 8A



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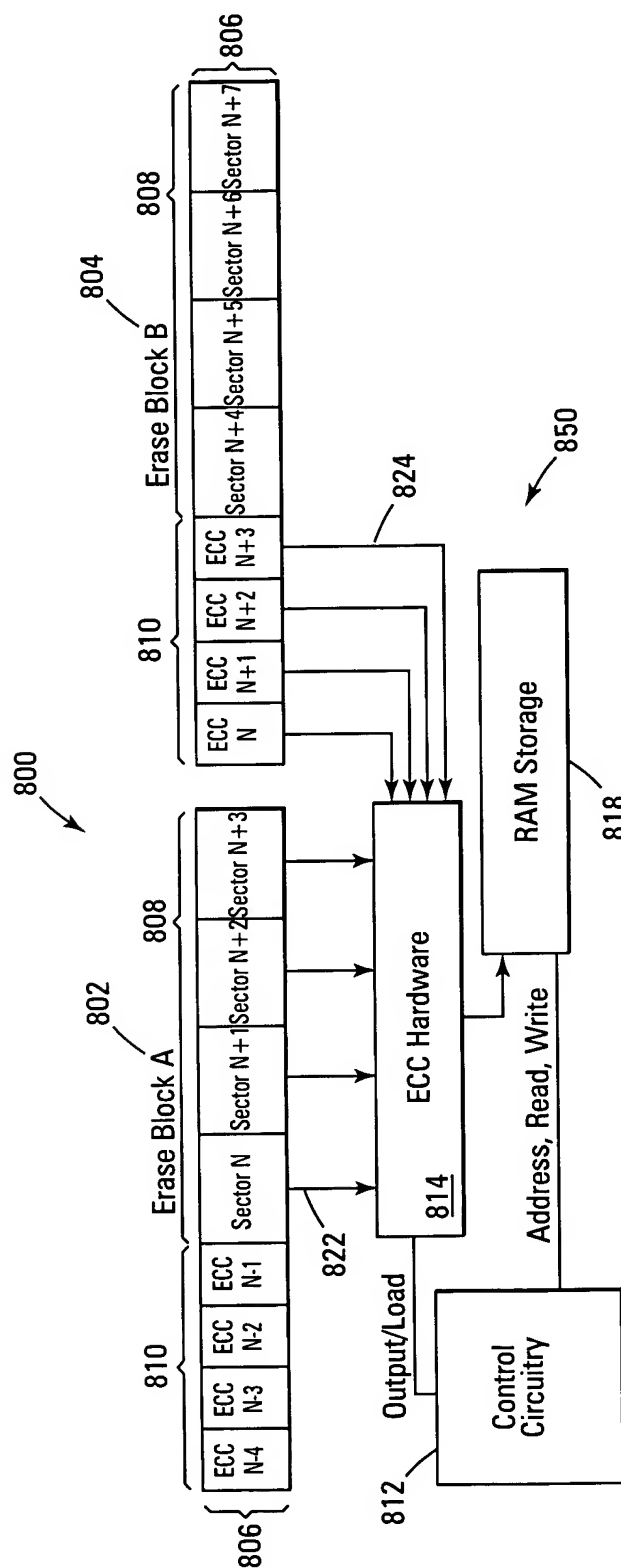


Fig. 8B